IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant	:	Huotari
App. No.	:	10/601,037
Filed	:	June 19, 2003
For	:	METHOD TO FABRICATE DUAL METAL CMOS DEVICES
Examiner	:	Christy Novacek
Art Unit	:	2822

CERTIFICATE OF MAILING

I hereby certify that this correspondence and all marked attachments are being deposited with the United States Postal Service as first-class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on

May 17, 2004
(Date)

Andrew N. Merickel, Reg. No. 53,317

AMENDMENT AND RESPONSE TO OFFICE ACTION

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

The present paper is submitted in response to the Office Action filed on February 18, 2004. Applicants respectfully request entry of the following amendments and consideration of the subsequent remarks.

Amendments to the Specification begin on page 2 of this paper.

Amendments to the Claims are reflected in the listing of claims which begins on page 3 of this paper.

Remarks/Arguments begin on page 7 of this paper.

AMENDMENTS TO THE SPECIFICATION

Please amend paragraph **[0053]** as indicated below.

[0053] The thick layer of conductive material 700 is etched where it is not masked. The etch is timed such that the dielectric 10 is not exposed and a thin barrier layer 200 is formed over one transistor region, for example the PMOS 50 region as shown in Figure 21. The remaining thick area under the mask forms a first gate electrode layer <u>750</u> ~~700~~ over the opposite transistor region, here the NMOS region 70, as illustrated in Figure 21. Typically, the thin barrier layer 200 is less than about 100 Å, more preferably from about 3 Å to about 50 Å, even more preferably from about 3 Å to about 30 Å.